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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/777,902	KOCH ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Nov 13, 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,4,6,8,9,11-22 and 24-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22 and 24* is/are allowed.

6)☒ Claim(s) *3, 4, 6, 8, 9, 11-21, and 25-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment submitted on Nov 13, 2008 was reviewed and considered with the following results:

The applicants' arguments/comments were persuasive with respect to the objection under 35 USC 132(a) described on page 3 of the previous Office Action. That objection has been withdrawn since the applicants' original Fig. 1 does show only a single capacitor coupled to a gate of a corresponding transistor (e.g. see capacitor 32 and transistor 48; and capacitor 34 and transistor 50).

Amended claim 22 overcame its rejection under 35 USC 112 as described on pages 3-4 of the previous Office Action. Therefore, that rejection has been withdrawn.

Amended claim 22 also overcame the rejection of claims 22 and 24 under 35 USC 103(a), with respect to Naganuma/Bui et al. This rejection has been withdrawn because the two capacitors of Bui et al. would provide a capacitive delay when turning the corresponding transistor on and off.

However, the applicants' arguments/comments, with respect to the other prior art rejections, were not persuasive. Therefore, these remaining rejections are described below, and associated comments are described later under the Response to Arguments section.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. The applicants are advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-4, 6, 8-9, 11-18, and 25-31 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma, in view of Bui et al. (Bui), both references cited in the previous Office Action. Fig. 1 of Naganuma shows a circuit comprising first terminal 1 understood to be connected to a voltage source (not shown) that provides input signal "a" transitioning between first/second levels (e.g. 5V and 0V as shown in Figs. 2(A) and 2(B)); driver 7 including first/second opposite conductivity type transistors $7_1/7_2$ (i.e. PFET 7_1 and NFET 7_2) with their respective control electrode b/c, and a (source/drain) path arranged to be switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold level (of each transistor); first/second transistor paths of $7_1/7_2$ are connected in series across opposite power supply terminals 5V and 0V; output terminal 10 is between the paths; circuitry $6_1/6_2$ is connected between first terminal 1 and control electrodes b/c for causing the first/second transistor paths to be in on and off states (e.g. when the voltage source provides input signal "a" at a first level (i.e. high), first transistor 7_1 is on and second transistor 7_2 is off; and when input signal "a" is at a second level (i.e. low), first transistor 7_1 is off and second transistor 7_2 is on).

However, Naganuma does not show or disclose circuitry $6_1/6_2$ with at least one voltage responsive switchable capacitor. Bui shows circuitry 802-808 in Fig. 8A receiving a single input signal IN, and providing a control signal to driver 809. Bui's circuitry provides a delay period determined by resistive elements 803,805 and capacitive elements 807,808. One of ordinary skill in the art knows this is one type of a time constant circuit. Each of Naganuma's inverter blocks 6_1 and 6_2 is also one known type of a time constant circuit (e.g. see column 4, lines 24-27), and Naganuma discloses these time constant circuits suppress output noise and excess current in the driver (e.g. see column 7, lines 62-65), which occurs when both transistors within the driver are conducting at the same time (e.g. see column 2, lines 31-37). Naganuma also discloses that although the simple time constant circuits can be inserted into the circuit, "embodiments are possible to modify in various ways without departing from the spirit of the invention" (e.g. see column 7, lines 62-68). Therefore, it would have been obvious to one of ordinary skill in the art to modify each of Naganuma's inverter blocks 6_1 and 6_2 by adding Bui's capacitors 807,808 to each inverter block's output b/c. With a pair of Bui's capacitors 807,808 coupled to output terminals b and c of Naganuma's inverters 6_1 and 6_2, respectively, the modified circuit will have the same type of structure as the applicants' own Fig. 1 with two minor exceptions (i.e. related to the series connection of a transistor and resistor within each inverter), and having two capacitors coupled in common to the gate of each corresponding transistor. For example, Naganuma's input terminal 1, first inverter 6_1 (with PFET 5_{11}, NFET 5_{12}, resistor R1, and output b), driver 7 (with first (PFET) transistor 7_1, second (NFET) transistor 7_2, and output 10), and second inverter 6_2 (with PFET 5_{21}, NFET 5_{22}, resistor R2, and output c); and first/second power supply terminals 5V/0V correspond to input terminal 39, first inverter 20

(with PFET 36, NFET 38, resistor 40, and output 28), driver 24 (with first (PFET) transistor 48, second (NFET) transistor 50, and output 26), and second inverter 22 (with PFET 42, NFET 44, resistor 46, and output 30); and first/second power supply terminals 16/18 shown in the applicants' own Fig. 1. With the addition of Bui's capacitors 807,808 to Naganuma's circuit, Bui's NFET 808 (connected to output b) and PFET 807 (connected to output c) correspond to the applicants' NFET 32 and PFET 34, respectively. Voltage responsive switchable capacitor NFET 808 will have its control electrode (i.e. gate) connected to the control electrode of first transistor 7_1 to receive the voltage (on b) applied to the gate of first transistor 7_1, and voltage responsive switchable capacitor PFET 807 will have its control electrode (i.e. gate) connected to the control electrode of second transistor 7_2 to receive the voltage (on c) applied to the gate of second transistor 7_2. Therefore, with this circuit configuration, the Naganuma/Bui circuit will be functionally equivalent to the applicants' own Fig. 1, and claims 3-4, 6, 8-9, 11-18, and 25-31 are rendered obvious. For example, with a corresponding set of Bui's switchable capacitors 807-808 coupled to each of b and c of Naganuma, the switching capacitor will have only one (PFET) voltage responsive switchable capacitor 807 (directly) connected to each corresponding control electrode, and only one (NFET) voltage responsive switchable capacitor 808 (directly) connected to each corresponding control electrode.

The following descriptions address the claimed limitations in more detail. Bui's NFET 808 configured capacitor will be open when the voltage at its gate (e.g. corresponding to output b or c of its respective inverter block) is below the capacitor configured transistor's threshold voltage (i.e. the voltage difference between the gate and drain/source connections is less than the NFET's threshold voltage), and have a finite capacitance when the voltage at its gate is above the

capacitor configured transistor's threshold voltage (i.e. the voltage difference between the gate and drain/source connections is greater than the NFET's threshold voltage). Similarly, Bui's PFET 807 configured capacitor will be open when the voltage at its gate (e.g. corresponding to output b or c of its respective inverter block) is above the capacitor configured transistor's threshold voltage (i.e. the voltage difference between the gate and drain/source connections is less than the PFET's threshold voltage), and have a finite capacitance when the voltage at its gate is below the capacitor configured transistor's threshold voltage (i.e. the voltage difference between the gate and drain/source connections is greater than the PFET's threshold voltage). Viewed in another manner, first (PFET) transistor 7_1 will be off when the voltage on b is higher than a threshold voltage equal to 5V-Vtp (with Vtp representing a threshold of a PFET), and first (PFET) transistor 7_1 will be on when the voltage on b is lower than that threshold voltage. Similarly, a PFET configured as a capacitor (e.g. Bui's 807) will be a substantially open circuit when the voltage across it (with respect to its gate and its source/ drain) is less than a threshold voltage equal to 5V-Vtp (with Vtp representing a threshold of a PFET), and it will be at a finite capacitance when the voltage across it is greater than that threshold voltage. Second (NFET) transistor 7_2 will be off when the voltage on c is less than a threshold voltage equal to 0V+Vtn (with Vtn representing a threshold of an NFET), and second (NFET) transistor 7_2 will be on when the voltage on c is higher than that threshold voltage. Similarly, an NFET configured as a capacitor (e.g. Bui's 808) will be a substantially open circuit when the voltage across it (with respect to its gate and its source/drain) is less than a threshold voltage equal to 0V+Vtn, and it will be at a finite capacitance when the voltage across it is greater than that threshold voltage. Therefore, it would be understood by one of ordinary skill in the art that the threshold voltages

are between the levels of the opposite power supply terminals, and each of these capacitor configured transistors (i.e. Bui's 807 and 808) function as one type of a switchable capacitor. Since only one corresponding PFET switchable capacitor is directly connected to the control electrode, and only one corresponding NFET switched capacitor is directly connected to the control electrode of each of transistors 7_1 and 7_2, independent claim 31 is rendered obvious. The modified Naganuma/Bui circuitry provides a slightly more complex time constant circuit, which can be used to more accurately set the delay time via the RC components within the circuitry. The time constant of each block can be more accurately controlled with this more complex circuitry, thus ensuring that both transistors within driver 7 will not be conducting at the same time (i.e. simultaneously on), and the dead time (i.e. when both switching transistors within the driver circuit are off) will be kept to a minimum. For example, one of ordinary skill in the art knows that excess current caused by both transistors within the driver circuit conducting at the same time is undesirable. Therefore, it is preferable to ensure the conducting transistor of the driver will be turned off before the other transistor within the driver will be turned on. However, too much dead (or blanking) time caused by both transistors being off at the same time is also undesirable for fast switching operations. Therefore, on/off operations of the driver transistors must be carefully, and accurately, controlled to ensure both transistors are temporarily off before the next transistor begins to conduct, and to also minimize that dead time. This control can be accomplished by utilizing Naganuma's inverter blocks 6_1 and 6_2, along with corresponding capacitor configured transistors 807,808 from Bui. Since each of power supply terminals 5V and 0V are a known type of a DC power supply terminal of the circuit, claim 3 is rendered obvious. Resistors R1 and R2, and each transistor within inverters 6_1 and 6_2, are resistive type elements,

and at least one of them is connected to supply current to their corresponding switchable capacitor in response to the voltage at first terminal 1, rendering claim 4 obvious. With a corresponding pair of Bui's switchable capacitors 807,808 coupled to each output of Naganuma's inverter blocks 6_1 and 6_2, the at least one switchable capacitor includes first/second voltage controlled switchable capacitors connected to delay coupling of the transitions to the control electrodes of the first/second transistors $7_1/7_2$, and claim 8 is rendered obvious. For example, the first and second capacitors can correspond to Bui's NFET 808 and PFET 807, respectively. Using NFET 808 connected to control electrode b of first transistor 7_1, and PFET 807 connected to control electrode c of second transistor 7_2, as examples, first capacitor 808 will have a finite capacitance on a first side of a first voltage threshold (i.e. a voltage greater than a threshold voltage of 0V+Vtn as previously described), and have a substantially open circuit on a second side of the first voltage threshold (i.e. a voltage less than a threshold voltage of 0V+Vtn as previously described); and second capacitor 807 will have a finite capacitance on a second side of a second voltage threshold (i.e. a voltage greater than a threshold voltage of 5V-Vtp as previously described), and have a substantially open circuit on a first side of the second voltage threshold (i.e. a voltage less than threshold voltage 5V-Vtp as previously described). Since a threshold voltage (e.g. 5V-Vtp) of a PFET is greater than the threshold voltage (e.g. 0V+Vtn) of an NFET, and with first capacitor 808 directly coupled between control electrode b and power supply terminal 0V, and second capacitor 807 directly coupled between control electrode c and power supply terminal 5V, claim 9 is rendered obvious. Claim 11 is rendered obvious for the same type of reasoning as previously described above with respect to claim 4, and Naganuma's first/second resistive elements R1/R2. First/second transistors $7_1/7_2$ are PFET/NFET,

respectively, and first/second capacitors 808/807 are NFET/PFET, respectively. The threshold voltage (e.g. 0V+Vtn) of first capacitor 808 is lower than threshold level (e.g. 5V-Vtp) of first transistor 7_1, and threshold voltage (e.g. 5V-Vtp) of second capacitor 807 is higher than threshold level (e.g. 0V+Vtn) of second transistor 7_{12}. This renders claim 12 obvious. Since Naganuma and Bui disclose the relationships between their inventions and integrated circuits (e.g. see column 1, lines 13-15 and column 1, lines 9-11, respectively), it would have been obvious to one of ordinary skill in the art that the at least one switchable capacitor and the PFET/NFET transistors of the driver are included on an integrated circuit chip, and the resistive element (i.e. R1, and/or R2) is a resistor, rendering claim 13 obvious. Circuitry 6_1,6_2,807,808 further includes first/ second inverters 6_1/6_2 each having input terminal 1 for simultaneously enabling the first/second inverters in response to voltage at first terminal 1, and an output terminal (b for inverter 6_1, and c for inverter 6_2). Output terminal b of first inverter 6_1 is connected to supply current via a first DC path (through 5_{11}) to first capacitor 808 and control electrode b of first transistor 7_1 to the exclusion of second capacitor 807 connected to control electrode c of second transistor 7_2; and output terminal c of second inverter 6_2 is connected to supply current via a second DC path (through 5_{22}) to second capacitor 807 and control electrode c of second transistor 7_2 to the exclusion of first capacitor 808 connected to control electrode b of second transistor 7_1, rendering claim 14 obvious. Since first/second transistors 7_1/7_2, first/ second inverters 6_1/6_2, and first/second capacitors 808/807 all comprise field effect transistors, claim 15 is rendered obvious. It would have been obvious to one of ordinary skill in the art, as previously described, to include all of the field effect transistors on an integrated circuit chip that includes first/second resistors R1/R2 respectively connected effectively with first/second

transistors $7_1/7_2$ and first/second inverters $6_1/6_2$, rendering claim 16 obvious. Since first/second resistors R1/R2 are respectively included in first/second inverters $6_1/6_2$, claim 17 is also rendered obvious. For the same type of reasoning as previously described above, and without repeating all of those various details, first/second inverters $6_1/6_2$ each comprise a PFET and an NFET (i.e. inverter 6_1 comprises PFET 5_{11} and NFET 5_{12}, and inverter 6_2 comprises PFET 5_{21} and NFET 5_{22}), and the inverters are driven in parallel by voltage on input terminal 1, rendering claim 18 obvious. First/second transistors $7_1/7_2$ are PFET/NFET transistors, respectively, and first/second capacitors 808/807 are NFET/PFET, respectively. First transistor 7_1 has a source drain path connection to positive power supply terminal 5V, and second transistor 7_2 has a source drain path connection to negative power supply terminal 0V, wherein these positive/negative power supply terminals are the first/second power supply terminals, respectively. First capacitor 808 has a first electrode connected to gate electrode b of first transistor 7_1 and a second electrode connected to negative power supply terminal 0V; and second capacitor 807 has a first electrode connected to gate electrode c of second transistor 7_2 and a second electrode connected to positive power supply terminal 5V. Therefore, claim 25 is rendered obvious for the same reasoning as applied to claim 12. Also by applying similar reasoning as previously described above, but interpreting the modified configuration described above (i.e. adding Bui's switchable capacitors 807,808 to output terminals b/c of Naganuma's inverters $6_1/6_2$) in a different manner, during a first interval (e.g. input signal a is high) first transistor 7_1 will be on and second transistor 7_2 will be off; and second capacitor 807, connected between 5V and output terminal b, will charge by current flowing from 5V to 0V through 807, 5_{12}, and R1, wherein first capacitor 808 (connected to output terminal c) will be off. This will occur because control electrode b (e.g. corresponding to

first voltage b) will have a first value (e.g. low), and the 5V coupled to the other side of second capacitor 807 will allow capacitor 807 to have a finite capacitance and charge, wherein control electrode c (e.g. corresponding to second voltage c) will also have the first value, but since the other side of first capacitor 808 is connected to a low (e.g. 0V), first capacitor 808 will be off. During a second interval (input signal a is low) first transistor 7_1 will be off and second transistor 7_2 will be on; and first capacitor 808, connected between 0V and output terminal c, will charge by current flowing from 5V to 0V through R2, 5_{21}, and 808, wherein second capacitor 807 (connected to output terminal b) will be off. This will occur because first voltage b will have a second value (e.g. high), and the 5V coupled to the other side of second capacitor 807 will prevent capacitor 807 from charging by switching it off, wherein second voltage c will have the second value, and since the other side of first capacitor 808 is connected to a low (e.g. 0V), second capacitor 808 will have a finite capacitance and be charged. One of ordinary skill in the art would understand that the timing (delay) related to the turning on and off of the first/second transistors will ensure both transistors are never conducting at the same time. However, during the transitioning periods between the first and second intervals, the driver transistor that is initially conducting will be turned off slightly before the other driver transistor will be turned on to minimize excess current (e.g. crowbar or shoot through). As an example, prior to the transition from the first to second interval, the following conditions are present: input signal "a" is high, first transistor 7_1 conducts, second transistor 7_2 is off, first capacitor 808 is off, and second capacitor 807 charges as described above. When input signal "a" transitions from a high to low level, gate electrode b of first transistor 7_1 will have an initial portion of the transitional period when its voltage will be low enough (i.e. less than 0V+Vtn) to keep capacitor 808 off (i.e.

open) and first transistor 7_1 on; during a second portion (when the voltage on b is above 0V+Vtn, but below 5V-Vtp), capacitor 808 will be on providing a finite capacitance, and first transistor 7_1 will still be on; and once the voltage on b is above 5V-Vtp (i.e. a third portion of the transitional period), capacitor 808 will still be on, but first transistor 7_1 will be off. The RC time delay related to inverters $6_1/6_2$, and their corresponding capacitors 807,808, will ensure both transistors are temporarily off before second transistor 7_2 begins to conduct, but with minimal dead time (i.e. when both transistors are off). Similar type operational periods will occur with respect to gate electrode c; and also when input signal "a" transitions from a low to high level. For example, as input signal "a" begins to decrease, the current path through 5_{12} and R1 of first inverter 6_1 turns off and transistor 5_{11} turns on, output terminal b of first inverter 6_1 becomes high, first capacitor 808 charges, and first transistor 7_1 turns off. Associated with the high to low transition of input signal "a", transistor 5_{22} eventually turns off and the current path through R2 and 5_{21} of second inverter 6_2 turns on, output terminal c of second inverter 6_2 becomes high, second capacitor 807 quits charging, and second transistor 7_2 turns on. Once these conditions are reached, the circuit will be in the second interval. The transition from the second interval to the first interval will be the opposite of those described above. Claims 26-30, and 6 are rendered obvious for the same type of reasoning as described above with respect to the other claims. For example, first/second transistors $7_1/7_2$ are PFET/ NFET transistors respectively; the opposite power supply terminals 5V/0V are first/second power supply terminals 5V/0V, respectively, wherein first power supply terminal 5V is connected to voltage 5V having a higher value than voltage 0V connected to second power supply terminal 0V; said at least one switchable capacitor 808,807 comprises PFET 807 having a gate electrode directly connected to gate electrode c of NFET second

transistor 7_2, and the source and drain electrodes of PFET capacitor 807 is connected to first power supply terminal 5V, wherein PFET capacitor 807 does not affect current flowing between input terminal 1 and the gate of PFET first transistor 7_1, rendering claim 28 obvious. Similar to claim 28 described above, but having said at least one switchable capacitor 808,807 comprising NFET 808, it has a gate electrode directly connected to gate electrode b of PFET first transistor 7_1, and the source and drain electrodes of NFET switchable capacitor 808 are connected to second power supply terminal 0V, wherein NFET capacitor 808 does not affect current flowing between input terminal 1 and the gate of NFET second transistor 7_2, thus rendering claim 29 obvious. [Note: Only one corresponding PFET switching capacitor is directly connected to the gate of the drive transistor, and only one corresponding NFET switching capacitor is directly connected to the gate of the drive transistor.] The circuit further comprises another switchable capacitor comprising PFET 807 having a gate electrode directly connected to gate electrode c of NFET second transistor 7_2, and the source and drain electrodes of PFET capacitor 807 being connected to first power supply terminal 5V, wherein PFET capacitor 807 does not affect current flowing between input terminal 1 and the gate of PFET first transistor 7_1. This renders claim 30 obvious.

Claims 19-21 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma/ Bui as applied to claim 18 above, and in view of the references by Yoshizawa et al. (Yoshizawa) and Takenaka. As previously described, the obvious modification of Naganuma's circuit with respect to Bui's switchable capacitors, reads on the limitations recited within claim 18, and closely correspond to the applicants' own Fig. 1 circuit. However, the first/second resistors of inverters $6_1/6_2$ are not connected in the same manner as recited within claim 19 (and

shown in the applicants' Fig. 1). However, it would have been obvious to one of ordinary skill in the art to reverse the series connection sequence of Naganuma's first resistor R1 and NFET 5_{12} within inverter 6_1, and also to reverse the series connection sequence of second resistor R2 and PFET 5_{21} in inverter 6_2. For example, Yoshizawa's Fig. 3 shows inverter 5 comprising PFET 35, NFET 28, and resistor 51 corresponding to Naganuma's inverter 6_1 with its PFET 5_{11}, NFET 5_{12} and resistor R1, respectively. In Fig. 2, Yoshizawa shows inverter 5 comprising PFET 34, NFET 27, and resistor 50 corresponding to the applicants' own inverter 20 with its PFET 36, NFET 38, and resistor 40. Yoshizawa discloses the "same operation as that in the circuit of Fig. 2 is conducted" with respect to Fig. 3 (e.g. see column 4, lines 34-35). Therefore, this is one example of reversing the positions of a resistor and transistor coupled in series, wherein the circuitry will still provide the same function. Another similar example is shown in Figs. 4B and 4C of Takenaka. However, unlike the Yoshizawa reference which shows a resistor coupled between the NFET and either an unlabeled low voltage (see Fig. 3) or the output terminal (see Fig. 2), Takenaka's examples show an unlabeled resistor coupled between an unlabeled PFET and either voltage VCC (Fig. 4B) or the output terminal (Fig. 4C). It is noted that Takenaka's Fig. 4B corresponds to Naganuma's inverter 6_2, and Fig. 4C corresponds to the applicants' inverter 22. Therefore, it would have been obvious to one of ordinary skill in the art to either replace the inverters of Naganuma with equivalent inverters (e.g. inverter 5 of Yoshizawa's Fig. 2 for Naganuma's inverter 6_1, and Takenaka's Fig. 4C inverter for Naganuma's inverter 6_2; or to reverse the series connections of the resistor with its corresponding transistor. With these modifications, first resistor R1 of Naganuma will be connected between the source drain path of NFET 5_{12} of first inverter 6_1 and output terminal b of first inverter 6_1, and second resistor R2 will

be connected between the source drain path of PFET 5_{21} of second inverter 6_2 and output terminal c of second inverter 6_2; or first resistor 50 of Yoshizawa's Fig. 2 will be connected between the source drain path of NFET 27 of first inverter 5 and the unlabeled output terminal of first inverter 5, and second resistor R of Takenaka will be connected between the source drain path of the unlabeled PFET of the second unlabeled inverter shown in Fig. 4C and its unlabeled output terminal, rendering claim 19 obvious. The positioning of the transistor and resistor within each inverter can obviously be reversed since they are connected in series between the corresponding inverter's output terminal and the inverter's power supply terminal. Therefore, this series connection forms a current path between those terminals, and since no output is taken from between those two elements (e.g. Naganuma's transistor 5_{12} and first resistor R1), their specific series arrangement is not critical. Bui's first/second capacitors 808/807 include NFET 808 and PFET 807, respectively. This, along with the same type of reasoning as applied to claim 12 above with respect to the threshold voltages and threshold levels, renders claim 20 obvious. NFET 808 will have a first (i.e. NFET) threshold (e.g. 0V+Vtn as previously described), and PFET 808 will have a second (i.e. PFET) threshold (e.g. 5V-Vtp as previously described). These thresholds are different, and one of ordinary skill in the art would understand they are also between the first/second levels. First NFET capacitor 808 will have a finite capacitance for a voltage above the second (i.e. NFET) threshold, and have a substantially open circuit for a voltage below the second threshold; and second PFET capacitor 807 will have a finite capacitance for a voltage below the first (i.e. PFET) threshold, and have a substantially open circuit for a voltage above the first threshold. One of ordinary skill in the art would understand the first threshold (e.g. corresponding to 5V-Vtp) is greater than the second threshold (e.g.

corresponding to 5V+Vtn) to ensure the driver transistors will be turned on and off without having both on at any one time, thus rendering claim 21 obvious.

Claims 3-4, 8, 14-18, and 31 also remain rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma (cited in the previous Office Action) in view of Love, a reference cited on IDS forms the applicant had previously submitted on Feb 13, 2004 and Nov 14, 2005. Fig. 1 of Naganuma shows a circuit comprising first terminal 1 understood to be connected to a voltage source (not shown) that provides input signal "a" transitioning between first/second levels (e.g. 5V and 0V as shown in Figs. 2(A) and 2(B)); driver 7 including first/second opposite conductivity type transistors $7_1/7_2$ (i.e. PFET 7_1 and NFET 7_2) with their respective control electrode b/c, and a (source/drain) path arranged to be switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold level (of each transistor); first/second transistor paths of $7_1/7_2$ are connected in series across opposite power supply terminals 5V and 0V; output terminal 10 is between the paths; circuitry $6_1/6_2$ is connected between first terminal 1 and control electrodes b/c for causing the first/second transistor paths to be in on and off states (e.g. when the voltage source provides input signal "a" at a first level (i.e. high), first transistor 7_1 is on and second transistor 7_2 is off; and when input signal "a" is at a second level (i.e. low), first transistor 7_1 is off and second transistor 7_2 is on). However, Naganuma does not show or disclose circuitry $6_1/6_2$ with at least one voltage responsive switchable capacitor. Love shows circuitry 68-80 in Fig. 3 receiving a single input signal IN, and providing a control signal to driver 90. Love's circuitry provides a delay period (e.g. RC time constant) determined by resistive element 72 and capacitive element 80. One of ordinary skill in the art knows this is one type of a time constant circuit. Each of Naganuma's inverter

blocks 6_1 and 6_2 is also one known type of a time constant circuit (e.g. see column 4, lines 24-27), and Naganuma discloses these time constant circuits suppress output noise and excess current in the driver (e.g. see column 7, lines 62-65), which occurs when both transistors within the driver are conducting at the same time (e.g. see column 2, lines 31-37). Naganuma also discloses that although the simple time constant circuits can be inserted into the circuit, "embodiments are possible to modify in various ways without departing from the spirit of the invention" (e.g. see column 7, lines 62-68). Therefore, it would have been obvious to one of ordinary skill in the art to modify each of Naganuma's inverter blocks 6_1 and 6_2 by adding Love's capacitor 80 to each inverter block's output b/c. With Love's capacitor 80 coupled to output terminals b and c of Naganuma's inverters 6_1 and 6_2, respectively, the modified circuit will have the same basic type of structure as the applicants' own Fig. 1 with three minor exceptions (i.e. related to the series connection of a transistor and resistor within each inverter; and the use of an NMOS transistor configured as a capacitor instead of a PMOS transistor). For example, Naganuma's input terminal 1, first inverter 6_1 (with PFET 5_{11}, NFET 5_{12}, resistor R1, and output b), driver 7 (with first (PFET) transistor 7_1, second (NFET) transistor 7_2, and output 10), and second inverter 6_2 (with PFET 5_{21}, NFET 5_{22}, resistor R2, and output c); and first/second power supply terminals 5V/0V correspond to input terminal 39, first inverter 20 (with PFET 36, NFET 38, resistor 40, and output 28), driver 24 (with first (PFET) transistor 48, second (NFET) transistor 50, and output 26), and second inverter 22 (with PFET 42, NFET 44, resistor 46, and output 30); and first/second power supply terminals 16/18 shown in the applicants' own Fig. 1. With the addition of Love's capacitor 80 to Naganuma's circuit, Love's NFET 80 (connected to output b) corresponds to the applicants' NFET 32. Voltage responsive

switchable capacitor NFET 80 will have its control electrode (i.e. gate) directly connected to the control electrode of first transistor 7_1 to receive the voltage (on b) applied to the gate of first transistor 7_1, and voltage responsive switchable capacitor NFET 80 will have its control electrode (i.e. gate) directly connected to the control electrode of second transistor 7_2 to receive the voltage (on c) applied to the gate of second transistor 7_2. Therefore, with this circuit configuration, the Naganuma/Love circuit will be effectively equivalent to the applicants' own Fig. 1. Love's NFET 80 configured capacitor will be open when the voltage at its gate (e.g. corresponding to output b or c of its respective inverter block) is below the capacitor configured transistor's threshold voltage (i.e. the voltage difference between the gate and drain/source connections is less than the NFET's threshold voltage), and have a finite capacitance when the voltage at its gate is above the capacitor configured transistor's threshold voltage (i.e. the voltage difference between the gate and drain/source connections is greater than the NFET's threshold voltage). This corresponds to waveform V76 shown in Love's Figs. 5a and 5b. For example, NFET 80 has a threshold Vtn, and when voltage V76 (corresponding to the voltage across the gate and drain/source of NFET 80) is below Vtn, the waveform shows minimal charge (corresponding to a substantially open circuit with respect to NFET 80). However, once V76 goes above Vtn due to the pull-up action of transistor 68 and resistor 72, the waveform shows a charging slope (corresponding to a finite capacitance that allows V76 to charge, with respect to the RC time constant of resistor 72 and capacitive element 80). First (PFET) transistor 7_1 will be off when the voltage on b is higher than a threshold voltage equal to 5V-Vtp (with Vtp representing a threshold of a PFET), and be on when the voltage on b is lower than that threshold voltage. Second (NFET) transistor 7_2 will be off when the voltage on c is less than a threshold

voltage equal to 0V+Vtn (with Vtn representing a threshold of an NFET), and be on when the voltage on c is higher than that threshold voltage. Therefore, it would be understood by one of ordinary skill in the art that the threshold voltages are between the levels of the opposite power supply terminals, and these capacitor configured transistors (i.e. corresponding to Love's 80) function as one type of a switchable capacitor. This renders claim 31 obvious. The modified Naganuma/Love circuitry provides a slightly more complex time constant circuit, which can be used to more accurately set the delay time via the RC components within the circuitry. For example, the time constant of each block can be more accurately controlled with this more complex circuitry, thus ensuring that both transistors within driver 7 will not be conducting at the same time (i.e. simultaneously on), and the dead time (i.e. when both switching transistors within the driver circuit are off) will be kept to a minimum. For example, one of ordinary skill in the art knows that excess current caused by both transistors within the driver circuit conducting at the same time is undesirable. Therefore, it is preferable to ensure the conducting transistor of the driver will be turned off before the other transistor within the driver will be turned on. However, too much dead (or blanking) time caused by both transistors being off at the same time is also undesirable for fast switching operations. Therefore, the on/off operations of the driver transistors must be carefully, and accurately, controlled to ensure both transistors are temporarily off before the next transistor begins to conduct, and to also minimize that dead time. This control can be accomplished by utilizing Naganuma's inverter blocks 6_1 and 6_2, along with corresponding capacitor configured transistors from Love. Since each of power supply terminals 5V and 0V are a known type of a DC power supply terminal of the circuit, claim 3 is rendered obvious. Resistors R1 and R2, and each transistor within inverters 6_1 and 6_2, are resistive type

elements, and at least one of them is connected to supply current to their corresponding switchable capacitor in response to the voltage at first terminal 1, rendering claim 4 obvious. With only one corresponding switchable capacitor 80 of Love directly coupled to each output of Naganuma's inverter blocks 6_1 and 6_2, the at least one switchable capacitor includes first/second voltage controlled switchable capacitors connected to delay coupling of the transitions to the control electrodes of the first/second transistors $7_1/7_2$, and claim 8 is rendered obvious. Circuitry 6_1,6_2,80,80 further includes first/second inverters $6_1/6_2$ each having input terminal 1 for simultaneously enabling the first/second inverters in response to voltage at first terminal 1, and an output terminal (b for inverter 6_1, and c for inverter 6_2). Output terminal b of first inverter 6_1 is connected to supply current via a first DC path (through 5_{11}) to first capacitor 80 and control electrode b of first transistor 7_1 to the exclusion of second capacitor 80 connected to control electrode c of second transistor 7_2; and output terminal c of second inverter 6_2 is connected to supply current via a second DC path (through 5_{22}) to second capacitor 80 and control electrode c of second transistor 7_2 to the exclusion of first capacitor 80 connected to control electrode b of second transistor 7_1, rendering claim 14 obvious. Since first/second transistors $7_1/7_2$, first/ second inverters $6_1/6_2$, and first/second capacitors 80/80 all comprise field effect transistors, claim 15 is rendered obvious. It would have been obvious to one of ordinary skill in the art, as previously described, to include all of the field effect transistors on an integrated circuit chip that includes first/second resistors R1/R2 respectively connected effectively with first/second transistors $7_1/7_2$ and first/second inverters $6_1/6_2$, rendering claim 16 obvious. Since first/second resistors R1/R2 are respectively included in first/second inverters $6_1/6_2$, claim 17 is also rendered obvious. For the same type of reasoning as previously described above, and without repeating

all of those various details, first/second inverters $6_1/6_2$ each comprise a PFET and an NFET (i.e. inverter 6_1 comprises PFET 5_{11} and NFET 5_{12}, and inverter 6_2 comprises PFET 5_{21} and NFET 5_{22}), and the inverters are driven in parallel by voltage on input terminal 1, rendering claim 18 obvious.

Claims 19 remains rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma/Love as applied to claim 18 above, and in view of the references by Yoshizawa et al. (Yoshizawa) and Takenaka. As previously described, the obvious modification of Naganuma's circuit with respect to Love's switchable capacitors, reads on the limitations recited within claim 18, and closely correspond to the applicants' own Fig. 1 circuit. Although Naganuma's resistors, and their corresponding transistor, are just the reverse of what is cited within claim 19, this claim is rendered obvious for the same type of reasoning previously described with respect to the rejection of claim 19 using the Naganuma/Bui/Yoshizawa/Takenaka references. For example, it would be obvious to one of ordinary skill in the art that the present configuration of Naganuma's first resistor R1 and NFET 5_{12}, of first inverter 6_1, can be reversed. These two components are coupled in series between node b and 0V, and whether the transistor be coupled between node b and resistor, or the resistor is coupled between node b and the transistor, will not affect the operation of these components within the circuit (e.g. see the equivalent inverter type circuits 5 shown in Figs. 3 and 2 of Yoshizawa).

Allowable Subject Matter

Claims 22 and 24 are allowed. There is presently no motivation to modify or combine any prior art reference(s) to ensure the paths of the first and second transistors are turned off

without any capacitive delay, as now cited within claim 22, upon which claim 24 depends.

Claims 1-2, 5, 7, 10 and 23 have been cancelled.

Response to Arguments

Although the applicants' arguments filed Nov 13, 2008 were persuasive with respect to the rejections of claims 22 and 24 under 35 U.S.C. 103(a) and the Naganuma/Bui et al. references, and those rejections have been withdrawn, the arguments are not persuasive with respect to the other prior art rejections described in the previous Office Action.

In response to the applicants' arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Naganuma shows/discloses inverters, each having a resistor within it, coupled to control the on/off operations of a corresponding transistor. Both Bui et al. and Love show examples of coupling at least one capacitor to the output of an inverter, wherein this inverter also has a resistor, or resistive device. One of ordinary skill in the art would understand the resistor/capacitor combination would provide one type of a delay circuit, and the delay would depend on the values of the resistor and capacitor. Although the applicants argue that the Love reference "does not supply any teaching or suggestion of providing a delay stage after or downstream of the inverter", it is noted the applicants also cite "capacitor 80, is provided between two inverter stages, 78,90." Whether each of 78 and 90 are called an "inverter stage" or just an inverter, it would be obvious to one of ordinary skill in the art that capacitor is indeed provided "after or downstream" of inverter 78.

The applicants' arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. The applicant argues that there is no reason to "separate the commonly connected capacitors 807, 808 of Bui." However, the rejections described in the previous Office Action, and this Office Action, do not separate the capacitors. Instead, the rejections describe a corresponding pair of both capacitors is coupled to each gate of Naganuma's corresponding transistors. For example, with Bui's pair of capacitors 807,808 coupled to gate b of Naganuma's transistor 7_1, there is only one single NFET capacitor 808 coupled between gate b and ground. Also, there is only one single PFET capacitor 807 coupled between gate b and the 5V power supply. Therefore, there is only one capacitor (of each type) coupled to the gate of the transistor.

The applicants also argue that it is not obvious to replace an NMOS capacitor with a PMOS capacitor. However, one of ordinary skill in the art would understand substantially functionally equivalent components can be used to replace one another. In this case, one MOS type capacitor (e.g. NMOS) is replaced with another known MOS type capacitor (e.g. PMOS). Also, which MOS configured capacitor is chosen can be determined by the time constant/delay (e.g. with respect to the rising or falling speed as the output of the inverter transitions between logic levels) to be obtained by the combination of the inverter and capacitor, and whether the MOS capacitor will be coupled between the inverter's output and ground, or between the inverter's output and the positive power supply.

Therefore, the rejections described in this Office Action are deemed proper with respect to the broadest reasonable interpretation of the claimed limitations, and of the prior art references cited.

THIS ACTION IS MADE FINAL. The applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln D. Donovan, can be reached on (571) 272-1988

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/T.L.E./

Examiner, Art Unit 2816

/Lincoln Donovan/

Supervisory Patent Examiner, Art Unit 2816